Effects of Dummy patterns and Substrate on Spiral Inductors for Sub- micron RF ICs

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Abstract — **In today's sub-micron CMOS technologies, dummy patterns are necessary to obtain the desired metal density for uniform etching. This paper shows the effect of the dummy patterns on the quality factor of the inductor. The effects of the polysilicon ground shield and p-doped substrate on inductor performance have also been investigated. As the distance of between dummy and inductor is increased, the quality factor is less influenced by eddy current loss due to dummy. And we can achieve Q = 13 @ 3GHz and L = 6.05 nH using patterned ground shield using slotted polysilicon layers in a commercial standard 0.18 μm CMOS technology.**

I. INTRODUCTION

Silicon, with its mature technology, low fabrication cost and high packing density is recognized as the only suitable material satisfying the needs of the rapidly growing communication market, i.e. IEEE 802.11a, Bluetooth, and WCDMA etc [1], [2]. One of the most beneficial merits of CMOS process is the continuous scaling down. Thus the sub-micron gate length MOSFETs can be used for low-noise applications at microwave frequencies (f_T = 50 GHz) [3].

The high-Q inductors in silicon technologies, however, have problems associated with the substrate loss and high resistive metal line. The substrate loss can be reduced by using high resistive silicon wafer which in turn introduces latch up problem for standard sub-micron CMOS process. Removing the lossy silicon substrate requires additional processing steps [4]. The problem with high resistive metal lines can be alleviated by using thick metal lines and/or low resistivity metal such as gold and copper.

In addition to these methods, other approaches such as layout optimization [5] or patterned ground shied techniques [6] have also been reported. These approaches are advantageous since additional process steps or special materials are not required.

In today's sub-micron CMOS technologies, dummy pattern structures are inserted to keep the different layers as planar as possible [7]. The dummy patterns are composed of many pieces of metal (M1-M6) and poly structures around the circuits as shown in Fig. 1. In radio frequency range, dummy patterns may cause some unexpected effect on inductance or Q of on chip inductor [7].

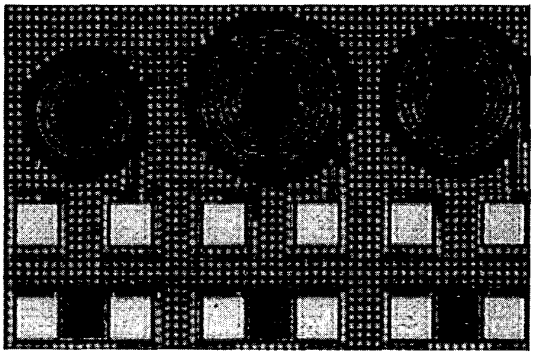

Fig. 1. Test patterns of spiral inductors with dummy patterns.

In this paper, we investigated the effect of the dummy patterns using two different distances between dummy and inductors. No dummy patterns are inside the inductors for protecting eddy current loss of inner dummy metals at high frequencies. Additionally, we compare two different types of inductors with normal inductor which has non p-doped substrate using additional masking layer. The first is patterned ground shield using slotted polysilicon layer. The second is p-doped substrate which is normally made in twin well process.

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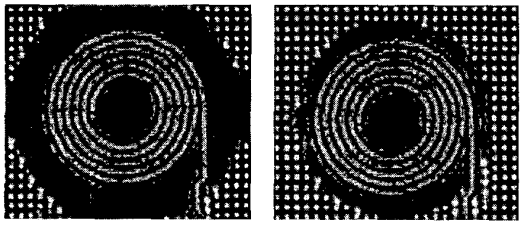
II. DESCRPTION OF IDUCTORS

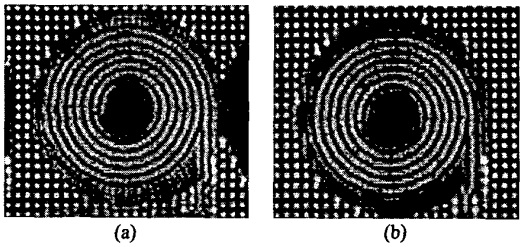
A conventional standard 0.18 μm 1P6M CMOS technology was used to fabricate various structures for circular spiral inductors. The last metal (M6, Al) is 2μm thick for decreasing metal loss. The p-bulk resistivity is 10Ω·cm, i.e. the same as non p-doped substrate.

To reduce the metal loss, we use multilevel (M6 and M5) wiring technology and connect them through a generous number of inter-level vias [8]. The turns of all the inductors are 5.5. Its expected inductance is 6.1 nH at 2 GHz. The inner diameter of the inductor is 90 μm, and



(a) (b)

Fig. 2. (a) 50μm distance dummy patterns from inductor. (b) 20μ distance dummy patterns from inductor.



(a) (b)

Fig. 3. (a) Inductor with patterned ground shields. (b) Inductor with p-doped substrate.

the inductor line width and spacing are fixed to be 10 μm and 2 μm, respectively.

Fig. 2 and Fig. 3 show the fabricated inductors. In fig. 2 (a), the distance between dummy patterns and the inductor is 50 μm, and Fig. 2 (b) has 20μm distance from the dummy to inductor. Fig. 2 (b) is the reference of all inductors. Dummy patterns are composed of various metals (M1-M6) and polysilicon whose size is 10x10 μm^2.

Fig. 3 (a) is inductor with patterned ground shield using slotted polysilicon layer which can prevent capacitive coupling to the lossy substrate and occurring eddy current in conductive substrate [4]. The polysilicon line patterned ground shield is orthogonal to the direction of current flow in the spiral. Fig. 3 (b) is inductor with p-doped substrate. The other inductors have non p-doped substrate (it's common type in inductor for reduce substrate loss) using additional masking layer - p-doped blocking layer - which diameter is bigger than inductor's by 20μm

III. RESULTS AND DISCUSSION

Two-port S-parameters were measured on the fabricated inductors using an HP 8501C network analyzer and Cascade Microtech RF probes. The measurement was taken for each inductor over frequency range of 500 MHz ~ 20 GHz. The "open" pad pattern without any inductor metal lines in Fig. 1 was also measured and used to remove the pad parasitics from measured S-parameters [9]. The measured two-port inductor parameters are determined uniquely from the Y-parameters converted from the de-embedded S-parameters: L= (1/ω)·Im(-1/Y12) and Q = - Im(Y11)/Re(Y11) [10]

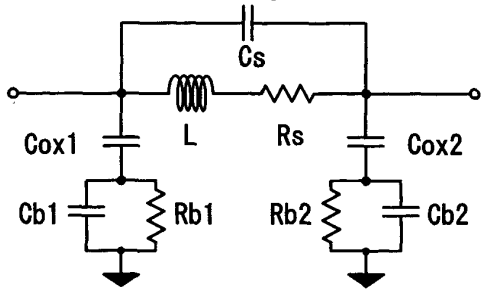


Fig. 4. Spiral inductor model.

Fig. 4 shows simple Π type inductor model. It is valid for inductor resonance frequency. Here Cb1, Cb2, Rb1, and Rb2 represent the lossy silicon substrate network. And Cox1, 2 represent the capacitive coupling underneath the inductor.

The inductor quality factor can be derived from the above model as follows:

$$Q = \frac{\omega Ls}{Rs} \times \frac{Rp}{Rp + [(\omega Ls / Rs)^2 + 1]Rs} \times \left(1 - \frac{Rs^2(Cs + Cp)}{Ls} - \omega^2 Ls(Cs + Cp)\right) \quad (1)$$

, where

$$Rp = \frac{1}{\omega^2 Cox^2 Rb} + \frac{Rb(Cox + Cb)^2}{Cox^2} \quad (2)$$

TABLE I

MODELS OF VARIOUS TYPE INDUCTORS

Inductor models	L (nH)	Rs (Ω)	Cs (fF)	Cox1 (fF)	Cox2 (fF)	Rb1 (Ω)	Rb2 (Ω)	Cb1* (fF)
50μm distance** dummy	6.15	6.0	13	97	116	1540	1330	23
20μm distance** dummy	6.05	6.6	15	101	114	1520	1310	25
PGS	6.05	6.1	17	72	75	47	43	370
P-doped sub	6.05	7.9	15	48	53	388	248	34

* Cb1 = Cb2 ** from the inductor

$$Cp = Cox\frac{1+\omega^2(Cox+Cb)CbRb^2}{1+\omega^2(Cox+Cb)^2Rb^2} \quad (3)$$

In (1), ωLs/Rs accounts for the magnetic energy stored and the ohmic loss in the series resistance. The second term in (1) is the resistor loss factor, and the last term in (1) is capacitor loss factor.

For requiring more insight, the Q of inductor is also regarded as follow [11]:

$$Q = Q_{metal} \| Q_{substrate} \quad (4)$$

, where Q_{metal} is the Q of ideal inductor which has no substrate loss and $Q_{substrate}$ is the quality factor of the substrate under resonance frequency.

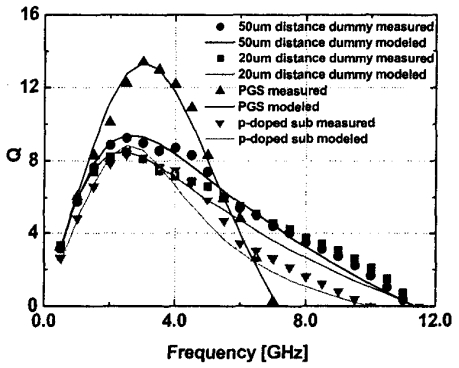


Fig. 5. Qs of the inductors with different distance dummy and the inductors with different substrate: polysilicon patterned ground shield (PGS), no p-doped blocking layer (p-doped sub.)

Because the value of Rb cannot be infinite in the silicon substrate, the $Q_{substrate}$ limit overall Q of the inductor additionally. And $Q_{substrate}$ can be higher value at the small value of Rb. Patterned ground shield can cause this effect. In the following frequency range, the limiting factor of the overall inductor Q is changing. Q_{metal} is dominant factor of the overall Q in f < f @ Q peak while $Q_{substrate}$ is dominant in frequency over f @ Q peak.

The Qs and inductance of the various types of inductors are shown in Fig. 5 and Fig. 6

The resonance frequency of inductor with p-doped sub is 10 GHz which is lower by 10% compared with reference inductor. Lowering the silicon substrate resistivity decreases Rb and increases Cb causing the Q roll-off to occur at a lower frequency and a reduction of the self-resonant frequency. And the inductor with 50 μm distance dummy does show higher Q than that the reference inductor with 20 μm distance dummy. The main reason is shown in Fig 7.

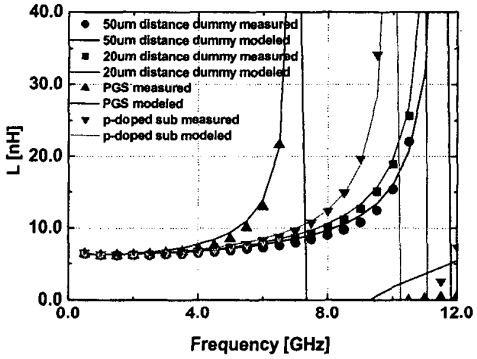


Fig. 6. Inductance of the inductors with different distance dummy and the inductors with different substrate

There are two induced current which disturb main magnetic flux of the inductor in dummy and substrate. According to Faraday's law, an eddy current is induced in the substrate underneath the inductor. To prevent the formation of substrate eddy current, a patterned ground shield is helpful [6]. In Fig. 5, tested inductor with the patterned ground shield does show noticeable Q enhancement, up to 52%. Quality factor plot of PGS inductor is observed to roll off much faster compared to other 3 inductors especially at high frequencies. This phenomenon is observed because the parasitic capacitance, Cb, is much larger compared to an unshielded inductor and dummy patterns near the inductor generate eddy current. And those current hinder the main flux of the

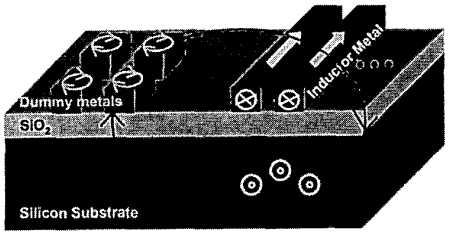


Fig. 7. Simplified current flow diagram of inductor with dummy patterns (Scale is not real)

inductor. So this effect is modeled by increasing series resistance. All types of inductor have nearly same inductance value. The all components in the model of the inductors are shown in Table 1.

IV. CONCLUSIONS

The effect of dummy pattern around the spiral inductor is investigated. The inductor with dummy separated by 50 μm shows higher Q than the inductor separated from dummy by 20 μm dummy. The former can improve the Q up to 12% for a 6.1nH spiral inductor. We deduce the following conclusion. The floating dummy patterns outside the inductor generate eddy current by Faraday's law. These current hinder the main flux of the inductor. This effect can be modeled by increasing series resistance and a slightly decreasing effective inductance. So carefully layout is needed in sub-micron CMOS process.

Two types of substrate are also investigated. The first substrate is the patterned ground shield. This shows high Q (= 13 @ 3GHz) in the expense of decreasing resonant frequency by 40%. The second is the p-doped substrate. Due to the low resistivity of the p-doped substrate, Rb is decreased and Cb is increased. This result causes reduction of the self-resonant frequency of inductor.

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